REMARKS

Reconsideration of the application is respectfully requested for the following reasons:

1. Amendments to Claims and Abstract

Claims 1 and 4 have been amended to include the subject matter of claims 3 and 6, namely that the deep trench is not only in communication with two different active areas, but also with adjacent bit lines (thereby making it easy to measure leakage currents involving the deep trench).

The abstract has been amended to place it in proper U.S. format and to correct a grammatical error.

Because the changes are all formal in nature, it is respectfully submitted that the changes do not involve new matter.

2. Rejection of Claims 1-6 Under 35 USC §102(b) in view of U.S. Patent No. 6,090,661 (Perng)

This rejection is respectfully traversed on the grounds that the Perng patent fails to disclose a deep trench structure that not only communicates with two different active areas, as recited in claim 1, but that also is respectively connected with two adjacent bit lines, so that the two adjacent bit lines are indirectly connected by means of the deep trench structure of the present invention. Instead, the Perng patent discloses a trench 19 formed between DRAM cells 1 and 3 and respectively connected to the same bit line (which overlies *word* lines 39 and 41). Similarly, trench 21 is formed between DRAM cells 5 and 7 connected to different *word* lines 43 but overlain by the same bit line.

More specifically, with reference to Figs. 1A and 1B of the Perng patent, a trench 19 is formed between DRAM cells 1 and 3 with capacitors 23 and 25 formed on the sidewall of the

trench 19, and a trench 21 is formed between DRAM cells 5 and 7 with capacitors 27 and 29 formed on the sidewall of the trench 21. **Word** (as opposed to **bit)** lines 39, 41, 43 and 45 contact gates of DRAM cells 1, 3, 5, 7, 9, 11, 13 and 15, such that word line 39 connects DRAM cells 1 and 9, word line 41 connects DRAM cells 3 and 11, word line 43 connects DRAM cells 5 and 13, while word line 45 connects DRAM cells 7 and 15. That is, DRAM cells 1 and 3 connect to two different **word** lines, respectively; and DRAM cells 5 and 7 connect to another two different **word** lines, respectively

As explained in **col. 6, lines 14-18** of the Perng patent, a **bit** line (not shown in the drawings) overlies cells 1, 3, 5, and 7 and electrically connects to region 17 (the bit line contact), while another bit line (also not shown) overlies cells 9, 11, 13 and 15 and electrically connects to regions 47 and 49. As a result, the DRAM cells 1 and 3, between which the deep trench 19 is formed, are overlain by the same bit line, and the cells 5 and 7, between which the deep trench 21 is formed, are overlain by the same bit line. Therefore, the Perng patent does not disclose or suggest a deep trench, which communicates with two active areas respectively connecting with two adjacent **bit** lines, as claimed by the present invention.

Because the Perng patent does not disclose all elements recited in amended claims 1, 2, 4, and 5, withdrawal of the rejection under 35 USC §102(b) is respectfully requested.

Having thus overcome each of the rejections made in the Official Action, expedited passage of the application to issue is requested.

Respectfully submitted,

BACON & THOMAS, PLLC

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By: BENJAMIN E. URCIA
Registration No. 33,805

BACON & THOMAS, PLLC
625 Slaters Lane, 4th Floor
Alexandria, Virginia 22314

Telephone: (703) 683-0500